



“Display” Design Office
Open Join-Stock Company

SPECIFICATION FOR RUGGEDIZED 3ATI LCD ASSEMBLY

Part Number: NVIT.433811.045

Part Number: NVIT.433811.045-01

Rev.8

28 Nov. 2017



Changes

| Revision | Date | Description |
|----------|------------|--|
| 6 | 12.04.2014 | Installation and dimensions drawing updated. |
| 7 | 12.08.2016 | Timing parameters of inputs interface updated. Installation and dimensions drawing updated. |
| 8 | 28.11.2017 | Outline drawing changed. Option without heater introduced. |



TABLE OF CONTENTS

- 1. GENERAL DESCRIPTION – P.3**
- 2. ENVIRONMENTAL CONDITIONS – P.4**
- 3. TECHNICAL PERFORMANCE – P.5**
- 4. CONNECTOR PINOUT AND SIGNALS DESCRIPTION – P.7**
- 5. TIMING PARAMETERS OF INRUTS INTERFACE – P.8**
- 6. INSTALLATION AND DIMENSIONS DRAWING – P.11**
- 7. CONTACT INFORMATION – P.13**



GENERAL DESCRIPTION

This specification defines a 3ATI Active Matrix Color LCD for use in extreme environmental conditions.

The LCD when installed in the next higher assembly (full display housing) shall withstand the environmental conditions defined in table 1.

The LCD assembly includes a 3ATI color LCD cell, attached drivers board with a single interface connector and laminated front AR / EMI / Heater glass (for NVIT.433811.045) or AR glass (for NVIT.433811.045-01).

ENVIRONMENTAL CONDITIONS

Table 1 – Environmental conditions for full LCD operation

| | | | |
|----------------------------------|--------|--|----------------|
| - Ambient temperature | | -55...+60°C | |
| - Short period operation (30min) | | +70°C | |
| - Storage temperature | | -55...+85°C | |
| - Altitude | | Up to 50,000 ft continuous; up to 70,000 ft for 2 minutes | |
| - Humidity | | Up to 95%, 40°C , 10 cycles of 24 hours | |
| - Shock | | 20 g for 11 ms | |
| - Acceleration | | Up to 7g for 1 minute | |
| Vibration | Mode 1 | g rms Hz | 1.8 10-2000 |
| | Mode 2 | g rms Hz | 2.83 10-500 |
| | Mode 3 | g Hz | 5 1-500 |
| - Sand and Dust | | + | |
| - Solar radiation | | 1125w/m ² , 3 cycles of 24 hours | |
| - Salt fog | | 2 cycles of 24 | |
| - HIRF | | 100V/m 10kHz...12,5GHz | |

TECHNICAL PERFORMANCE

Table 2 – LCD parameters and technical performance

| Parameter | Value |
|---|--------------------------------------|
| Active area, mm | 56.16 x 56.16 |
| Pixel resolution | 480x480 |
| Display colors | 262k(6bit/color) |
| Pixel size, mm | 0.117 x 0.117 |
| Viewing angles -Horizontal | ±80° |
| -Vertical | ±80° |
| Input interface | CMOS 6 bit |
| Supply voltage, VDD | +3,0 ^{+0.6} _{-0.3} |
| Contrast, min | 360:1 |
| Optical transmission (at normal to LCD) | At least 4.5% for white light |
| Heater resistance and power | 16±2.5 Ohm, not more than 7W rms |
| “Ready” time: | |
| - in normal temp. conditions | ≤ 2 sec |
| - in low temp. conditions | ≤ 5 min |
| Specular reflection at 30° | ≤ 1% |
| Diffuse reflection at 30° | ≤ 0.1% |
| Switching times at all temperature range: | |
| - TON | ≤ 60ms |
| - TOFF | ≤ 40ms |

For additional parameters see specification for Ortustech LCD COM37H3M83ULC.

Display Element Defects

Definition: failed-ON element is a single addressable element which is permanently or sporadically in the ON or partially ON condition when it has not been selected ON. An element is failed-ON when if it is selected off and its luminance is more than twice that of an adjacent selected OFF element.

A failed-OFF element is a single addressable element which is permanently or sporadically in the OFF or partially OFF condition when it has not been selected OFF. An element is failed-Off when it is selected ON and its luminance is less than 50% that of an adjacent selected ON element.

The maximum number of failed-ON elements plus failed-OFF elements shall be 3.

Element Defect Clusters

An element defect cluster is defined as two or more adjacent failed sub-pixels. There shall be no cluster defects within the active viewing area.

Spherical/Aspherical Defects

Table 1 indicates the requirements that apply to all spherical/aspherical defects visible on the display surface, including bubbles, digs, blotches and blemishes.

Table 3: Spherical/Aspherical Defect Criteria

| Spot Size | Allowed Quantity | Comments |
|-------------|------------------|----------|
| >1.0mm | 0 | - |
| 0.5 - 1.0mm | 4 | - |
| <0.5 mm | No limit | - |

Elongated Defects

Table 2 indicates the requirements that apply to all elongated defects visible on the display surface, including scratches and fibers.

Table 4: Elongated Defect Criteria

| Width | Cumulative Max Length | Max Allowable | Minimum Separation |
|-------------------|-----------------------|---------------|--|
| >0.25 mm | 0 | None | 0 |
| 0.10 - 0.25 mm | 12.5 mm | 1 | N/A |
| 0.05 mm - 0.10 mm | 25.4 mm | 4 | Minimum separation distance of 12.5 mm |
| <0.05 mm | No limit | No limit | N/A |

CONNECTOR PINOUT AND SIGNALS DESCRIPTION

| No. | Symbol | Function |
|-----|--------|---|
| 1 | VSS | Ground |
| 2 | VSS | Ground |
| 3 | VDD | Power supply input. |
| 4 | VCCIO | Logic Interface Power supply input. |
| 5 | VSS | Ground |
| 6 | RESETB | System reset signal input.(Lo: active) |
| 7 | HSYNC | Horizontal sync signal input. (Negative polarity) |
| 8 | VSYNC | Vertical sync signal input.(Negative polarity) |
| 9 | CLK | Clock input for display. (Data Input on the falling edge) |
| 10 | VSS | Ground |
| 11 | D00 | Display data input for (B). 00h for black display D00:LSB D05:MSB Driver IC carries out gamma conversion internally. |
| 12 | D01 | |
| 13 | D02 | |
| 14 | D03 | |
| 15 | D04 | |
| 16 | D05 | |
| 17 | D10 | Display data input for (G). 00h for black display D10:LSB D15:MSB Driver IC carries out gamma conversion internally. |
| 18 | D11 | |
| 19 | D12 | |
| 20 | D13 | |
| 21 | D14 | |
| 22 | D15 | |
| 23 | D20 | Display data input for (R). 00h for black display D20:LSB D25:MSB Driver IC carries out gamma conversion internally. |
| 24 | D21 | |
| 25 | D22 | |
| 26 | D23 | |
| 27 | D24 | |
| 28 | D25 | |
| 29 | VSS | Ground |
| 30 | DE | Input data effective signal. (It is effective for the period of "H") |
| 31 | STBYB | Standby signal (Lo:Standby operation,Hi:Normal operation) |
| 32 | TEST1 | Connect to Ground. |
| 33 | NC | OPEN |
| 34 | NC | OPEN |
| 35 | NC | OPEN |
| 36 | NC | OPEN |
| 37 | TEST2 | Connect to Ground. |
| 38 | BLH | LED drive power source. (Anode side) |
| 39 | BLL | LED drive power source. (Cathode side) |

Note: contacts 38 and 39 are not used, should be left open.

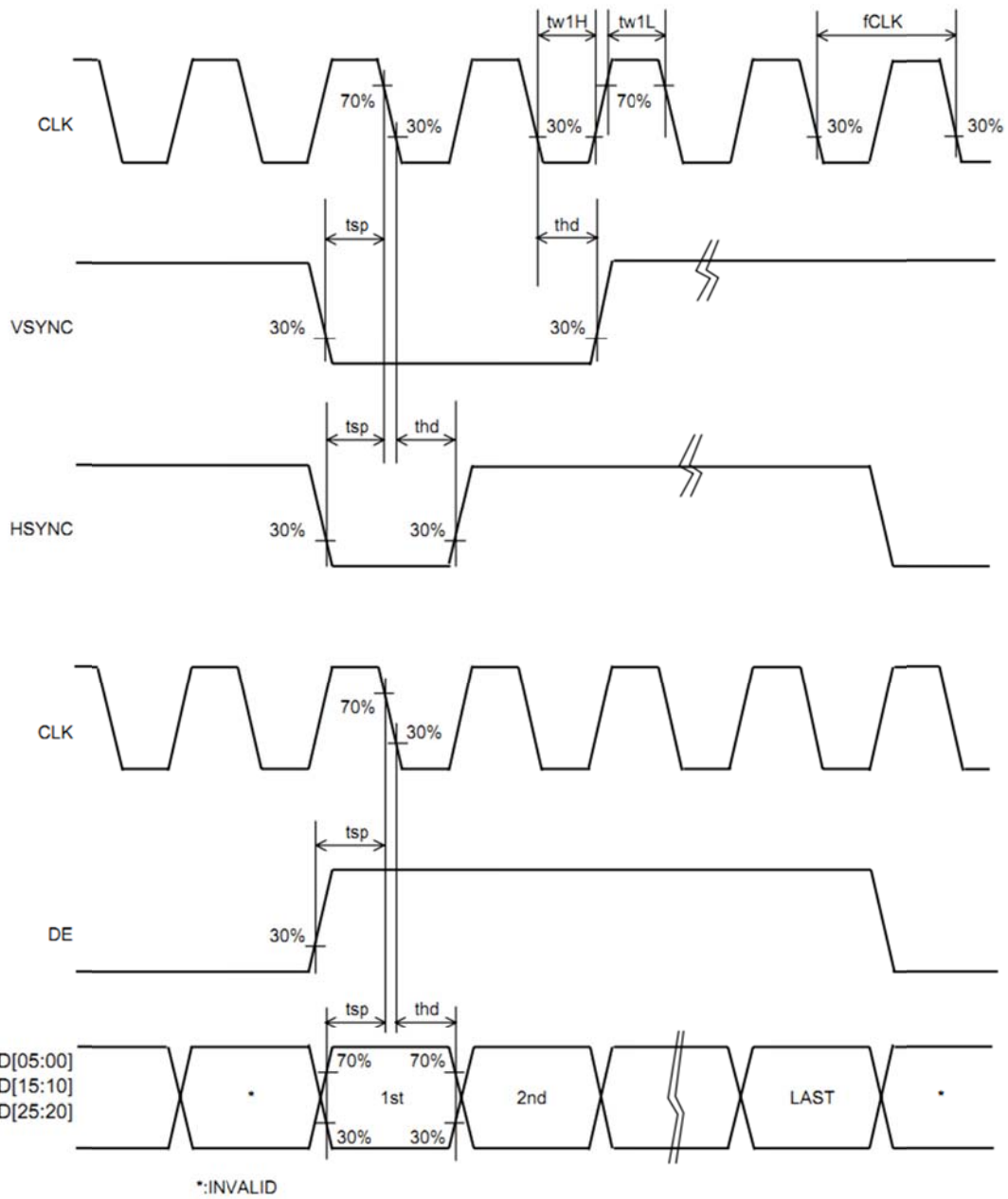
LCD connector type: FH23-39S-0.3SHW(05) made by Hirose Electric.

Heater connection is via flying wires soldered to the Heater bus-bars shown in INSTALLATION AND DIMENSIONS DRAWING (page 11).

TIMING PARAMETERS OF INPUTS INTERFACE

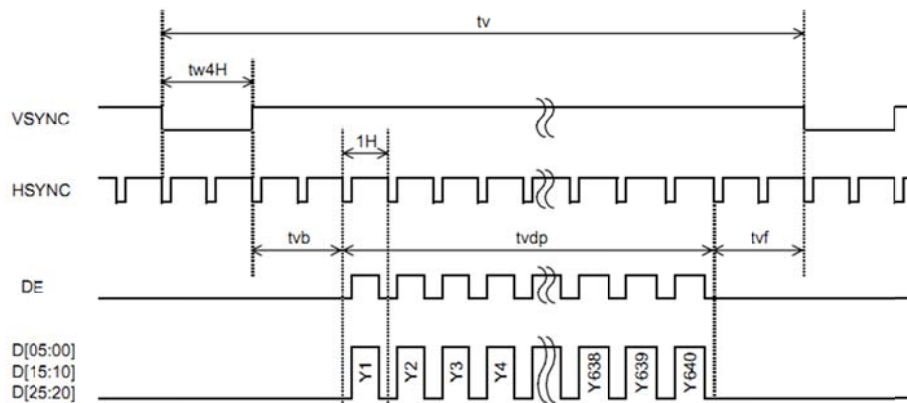
(Unless otherwise noted, Ta=25°C, VDD=3.0V, VCCIO=1.8V, VSS=0V)

| Item | Symbol | Condition | Rating | | | Unit | Applicable terminal |
|-----------------|--------|-------------------|--------|------|-----|------|---|
| | | | MIN | TYP | MAX | | |
| CLK frequency | fCLK | | 18 | 19.8 | 27 | MHz | CLK |
| CLK Low period | tw1L | 0.3×VCCIO or less | 10 | -- | -- | ns | |
| CLK High period | tw1H | 0.7×VCCIO or more | 10 | -- | -- | ns | |
| Setup time | tsp | | 10 | -- | -- | ns | CLK, VSYNC, HSYNC, DE, D[05:00], D[15:10], D[25:20] |
| Hold time | thd | | 10 | -- | -- | ns | D[05:00], D[15:10], D[25:20] |

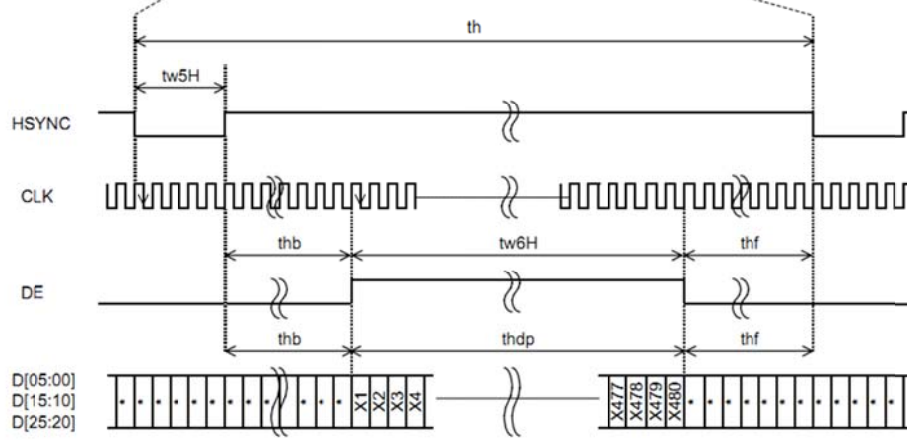


| Item | Symbol | Rating | | | Unit | Applicable terminal |
|-----------------------------|--------------|--------|------|------|------|---------------------------------------|
| | | MIN | TYP | MAX | | |
| CLK Frequency | fCLK | 18 | 19.8 | 27 | MHz | CLK |
| VSYNC Frequency | Note fVSYNC | 54 | 60 | 66 | Hz | VSYNC |
| VSYNC Cycle | tv | 646 | 650 | 700 | H | VSYNC,HSYNC |
| VSYNC Pulse Width | tw4H | 2 | 3 | 50 | H | |
| Vertical Back Porch | tvb | 2 | 3 | 50 | H | VSYNC,HSYNC,DE, |
| Vertical Front Porch | tvf | 2 | 4 | 50 | H | D[05:00],D[15:10],D[25:20] |
| Vertical Display Period | tvd | -- | 640 | -- | H | |
| HSYNC frequency | fHSYNC | -- | 39.0 | 50.0 | kHz | HSYNC |
| HSYNC Cycle | th | 504 | 508 | 630 | CLK | CLK,HSYNC |
| HSYNC Pulse Width | tw5H | 5 | 10 | 140 | CLK | |
| Horizontal Back Porch | thb | 5 | 10 | 140 | CLK | CLK,HSYNC,DE, |
| Horizontal Front Porch | thf | 5 | 8 | 140 | CLK | D[05:00],D[15:10],D[25:20] |
| Horizontal data start Point | tw5H+thb | 19 | -- | 145 | CLK | |
| Horizontal Blanking Period | tw5H+thb+thf | 24 | -- | 150 | CLK | |
| DE Pulse Width | tw6H | -- | 480 | -- | CLK | CLK,DE |
| Horizontal Display Period | thdp | -- | 480 | -- | CLK | CLK,DE, D[05:00],D[15:10],D[25:20] |

-Vertical Timing

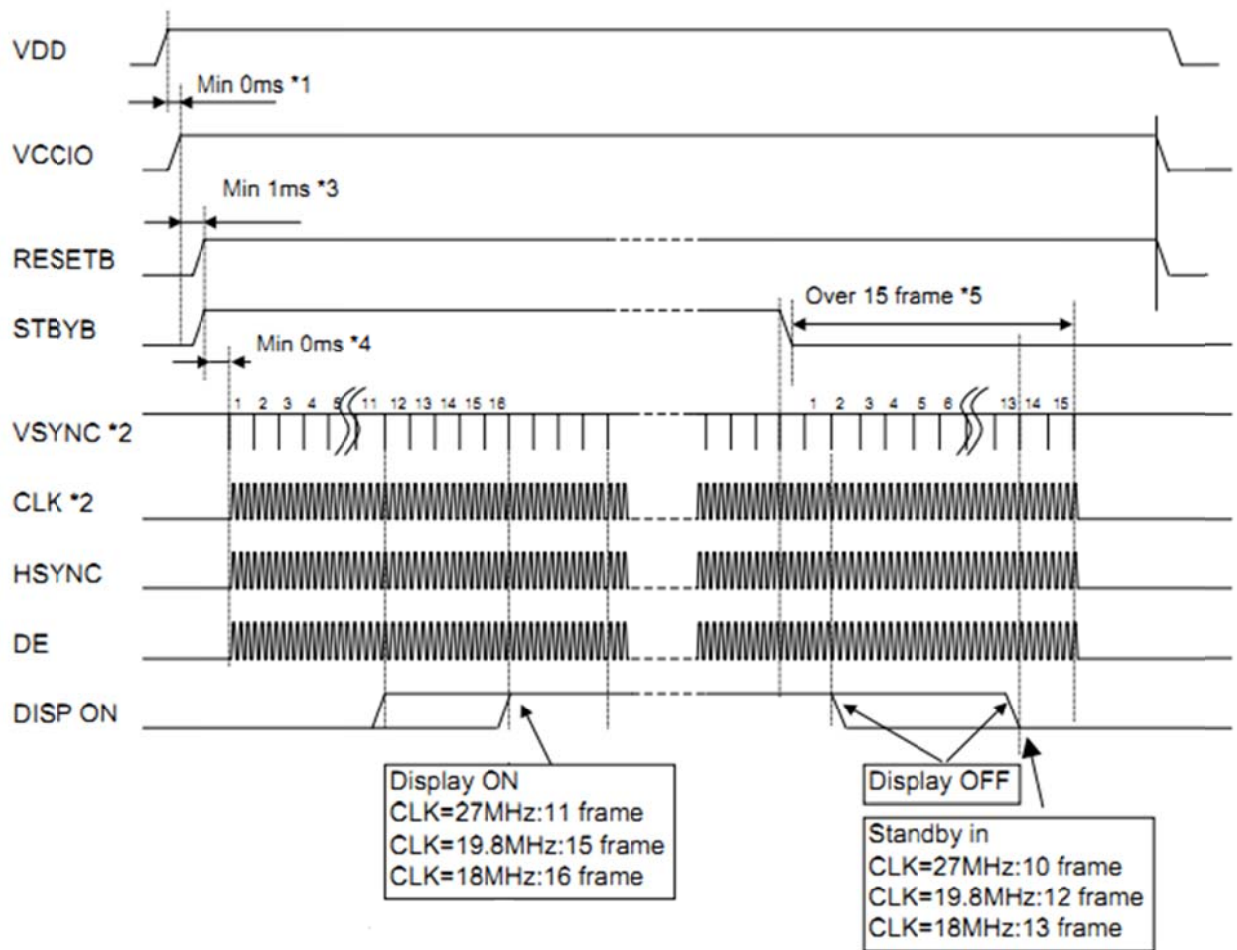


-Horizontal Timing



Note: For image creation the video signal should starts from pixel with coordinates X:0; Y:160 (see INSTALLATION AND DIMENSIONS DRAWING).

All pixels in coordinates' range from X:0;Y:0 up to X:479;Y:159 should be switched off.



*1 Please start up VDD and VCCIO at the same time or in order of VDD --> VCCIO.

*2 CLK is used for Gate array CLK on FPC.
 VSYNC is used for Gate array's inside counter.
 It becomes the operation after CLK ,VSYNC input.

*3 After the power supply, Please execute RESETB.

*4 There is no regulations at time until each signal is supplied from RESETB"H"
 But meanwhile, It is necessary to fix each signal to "H"or"L".

*5 It is necessary to supply VSYNC and CLK for 15 frames or more from STBYB "L" to
 turning off the power supply without leaving the afterimage.



INSTALLATION AND DIMENSIONS DRAWING NVIT.433811.045-01

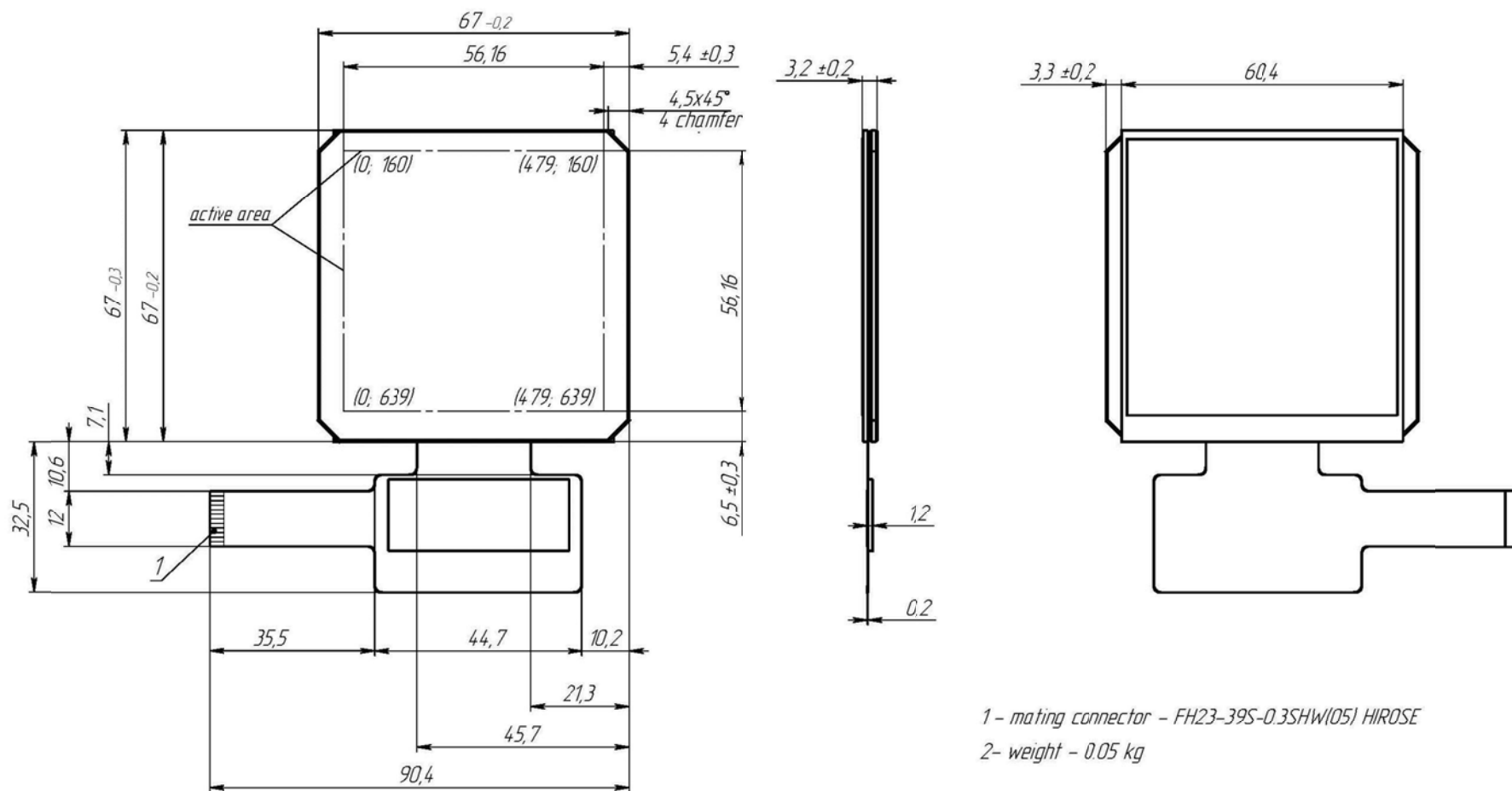


Figure 2: Installation and dimensions drawing NVIT.433811.045-01

Note: version without heating layer, AR glass only



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The Specification can be changed without notification.